ENFORCEMENT OF THE SEMICONDUCTOR INTEGRATED CIRCUITS LAYOUT-DESIGN

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Abstract

In today world, integrated circuit is used in most of the devices. IC layout design innovation of integrated circuit is protected under Semiconductor Integrated Circuits Layout Design Act 2000. IC Layout design depicts physical connection between two components (transistors) of the IC.Layout-design means a layout of transistors and other circuitry elements and includes lead wires connecting such elements and expressed in any manner in a semiconductor integrated circuit as per section 2(h) of the Semiconductor Integrated Circuits Layout-Design Act, 2000.The registration procedure includes: filing of application; accepted application advertised (14 days); opposition (3 months); counter-statement (2 months); registration of a layout-design for 10 years. The owner of registered layout-designs has the exclusive right to use the layout-design in any article/good/product/device and get relief from the court against any infringement in this respect. The right of registered user to take proceedings against infringement as subject to any agreement subsisting between the parties, as per section 28 of the Semiconductor Integrated Circuits Layout-Design Act 2000. As per official registry record limited registration application comes for registration as making a copy of the registered IC Layout design is not so easy task.

Keywords: Semiconductor Integrated Circuits Layout-Design; procedures; Registration; Semiconductor Integrated Circuits Layout-Design Act 2000; Enforcement.

Introduction

As we are aware that semiconductor technology and ICT industry is at the origin of their development thus it is imperative to discuss this Intellectual property in the realm of today's digital economy. The invention of semiconductors led to the rapid rise of personal computers. The semiconductor industry itself has been growing for more than four decades. Semiconductor Integrated circuits are fabricated from a complex series of layers of semiconductors, metals, dielectrics and other materials on a substrate.IC Layout is a drawing that depicts the physical connections between components. It shows the exact physical locations of every component on the PCB and shows the physical wires (traces) that connects them together. This IC layoutdrawing is used by manufacturer to fabricate the PCB.It is possible to copy such a layout design for a fraction of that cost. Copy of such intellectual work in forms of new IC layout, can discourage creativity or innovation in the field of integrated circuit layout.

History

The terms semiconductor integrated circuit means a product having transistors and other circuitry elements which are inseparably formed on a semiconductor material or an insulating material or inside the semiconductor material and designed to perform an electronic circuitry function as per Section 2(r) of the Semiconductor Integrated Circuits Layout-Design Act, 2000.

Kilby recorded his initial ideas concerning the integrated circuit in July 1958, successfully demonstrating the first working example of an integrated circuit on 12 September 1958. However, Kilby's invention was a hybrid integrated circuit (hybrid IC) which was made of germanium.Noyce's monolithic IC put all components on a chip of silicon and connected them with copper lines. Noyce's monolithic IC was fabricated using the planar process, developed in early 1959 by his colleague Jean Hoerni. Modern IC chips are based on Noyce's monolithic IC.NASA's Apollo Program was the largest single consumer of integrated circuits between 1961 and 1965.

The first microprocessorchip was developed in 1971. By the early 1980s, developers could fabricatechips containing more than 100,000 transistors. From the 1970s through to the1990s, the chip has become so ubiquitous that it is found in products rangingfrom automobiles to refrigerators to personal computers and a vast variety of "personal electronics."

Mask work exclusive rights were first granted in the US under Semiconductor Chip Protection Act(SCPA) of 1984established a new typeof intellectual property protection for mask works that are fixed in semiconductor chips.The United States Code defines a mask work as "a series of related images, however fixed or encoded, having or representing the predetermined, three-dimensional pattern of metallic, insulating, or semiconductor material present or removed from the layers of a semiconductor chip product, and in which the relation of the images to one another is such that each image has the pattern of the surface of one form of the semiconductor chip product".

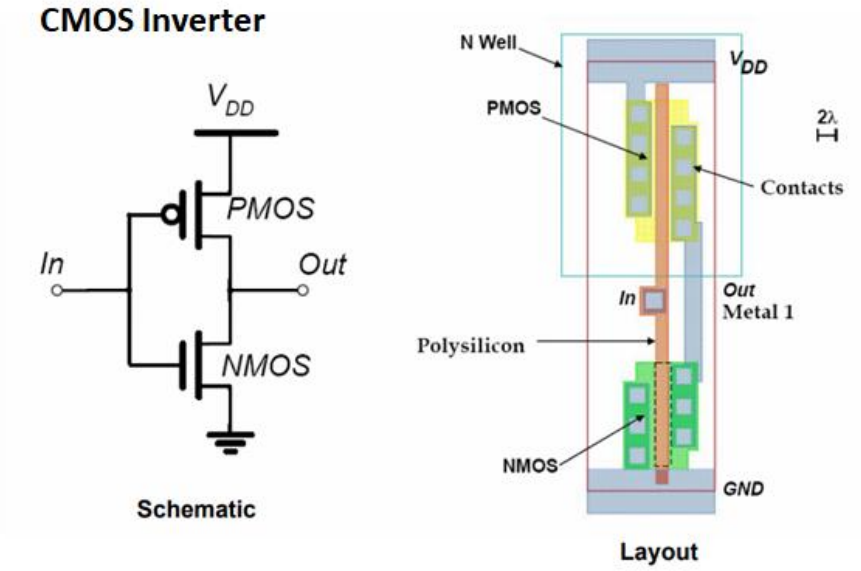
Integrated circuit and Integrated circuit layout:

An integrated circuit is thus formed when a miniaturized electrical circuit is embodied within a chip. All the active and passive components are created in the semiconductor wafer during the fabrication process itself and are therefore inseparable once the chip has been produced.

Integrated circuit layout is also known IC layout, IC mask layout, or mask design or integrated circuit topography.Layout-design means a layout of transistors and other circuitry elements and includes lead wires connecting such elements and expressed in any manner in a semiconductor integrated circuit as per section 2(h) of the Semiconductor Integrated Circuits Layout-Design Act, 2000 (hereinafter referred to as the "Act").

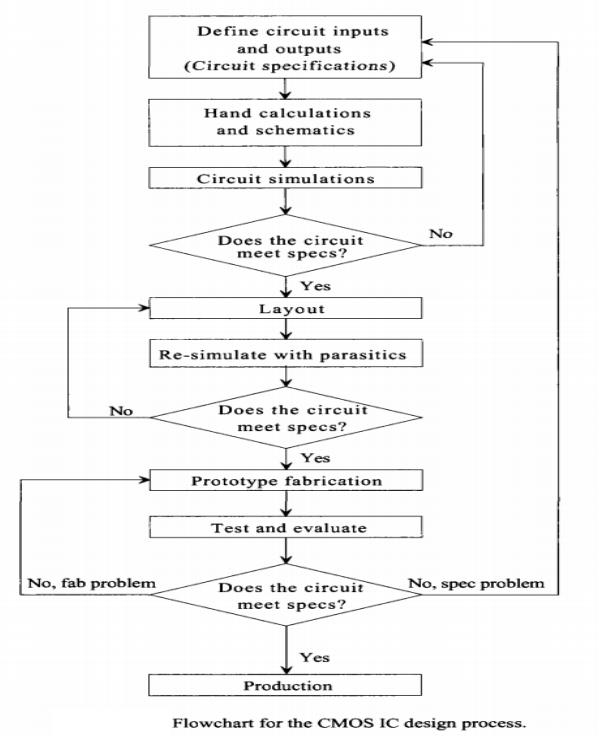
A layout-design is defined in Article 2(i) of the Treaty on Intellectual Property in Respect of Integrated Circuits (IPIC Treaty), as incorporated into the TRIPS Agreement, is the three-dimensional disposition, however expressed, of the elements at least one of which is an active elementor all of the interconnections of an integrated circuit, or such a three-dimensional disposition prepared for an integrated circuit intended for manufacture. In other words, a layout design is the three-dimensional layout of an integrated circuit, i.e. the arrangement in a chip (usually made of semiconductor crystal) of active and passive electronic components.

Washington Treaty (1989) provides protection for the layout designs (topographies) of integrated circuits. The Treaty has not yet entered into force, but has been ratified.

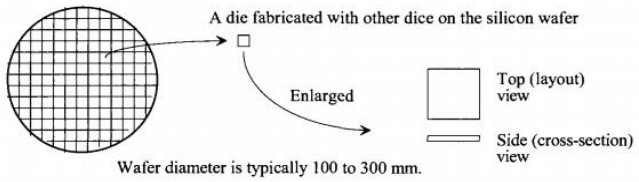


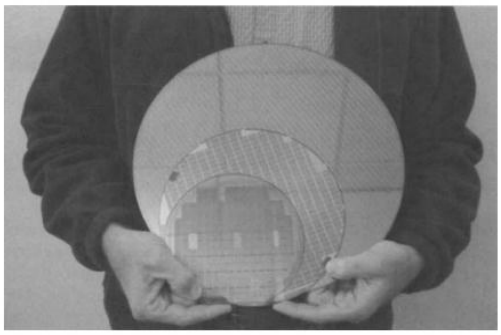
Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

The CMOS IC Design Process:The CMOS circuit design process consists of defining circuit inputs and outputs, handcalculations, circuit simulations, circuit layout, simulations including parasitic,re-evaluation of circuit inputs and outputs, fabrication, and testing. A flowchart of thisprocess is shown in Fig. The task of laying out the IC is often given to a layout designer. However, it isextremely important that the engineer can lay out a chip (and can provide direction to thelayout designer on how to layout a chip) and understand the parasitic involved in the layout.



Flowchart for the CMOS IC design process.



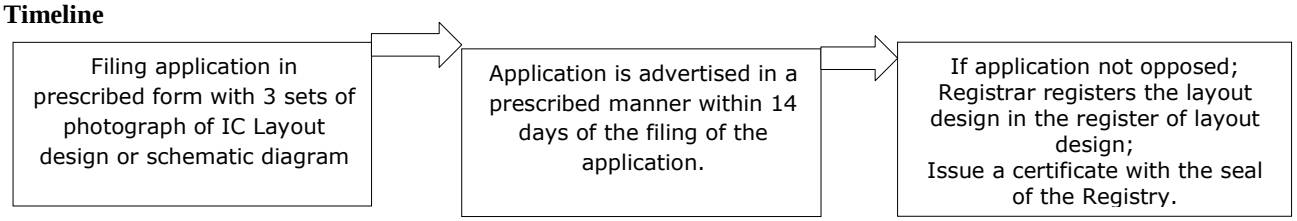


CMOS integrated circuits are fabricated on thin circular slices of silicon called wafers.Each wafer contains several (perhaps hundreds or even thousands) of individual chips or"die".

Criteria for registration: a layout-design which is original or which has not been commercially exploited anywhere in India or in a convention country; or which is inherently distinctive; or which is inherently capable of being distinguishable from any other registered layout design.

A layout-designwhich is not original or which has been commercially exploited anywhere in India or in a convention country; or which is not inherently distinctive; or which is not inherently capable of being distinguishable from any other registered layout design such layout-designs have been prohibited of registration undersection 7 of the Semiconductor Integrated Circuits Layout-Design Act, 2000.

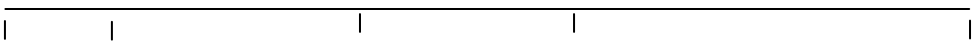
Timeline



File application

Months Advertised

(0) (14 days) (Opposition 3 M)(Counter: 2 M)(Not opposed and Register)



The registration cycle includes:

1) Filing of application by the creator of the layout-design at the SICLD Registry.

2) The acceptance of application.

- Registrar may accept, refuse the application or accept with some modifications.

  3) The accepted applications shall be advertised within 14 days of acceptance.

  4) Any opposition to the advertisement can be filed within 3 months from the date of advertisement.

  5) The counter-statement to the notice of opposition, if any, to be filed within 2 months from the date of receipt of copy of notice of opposition from the Registrar.

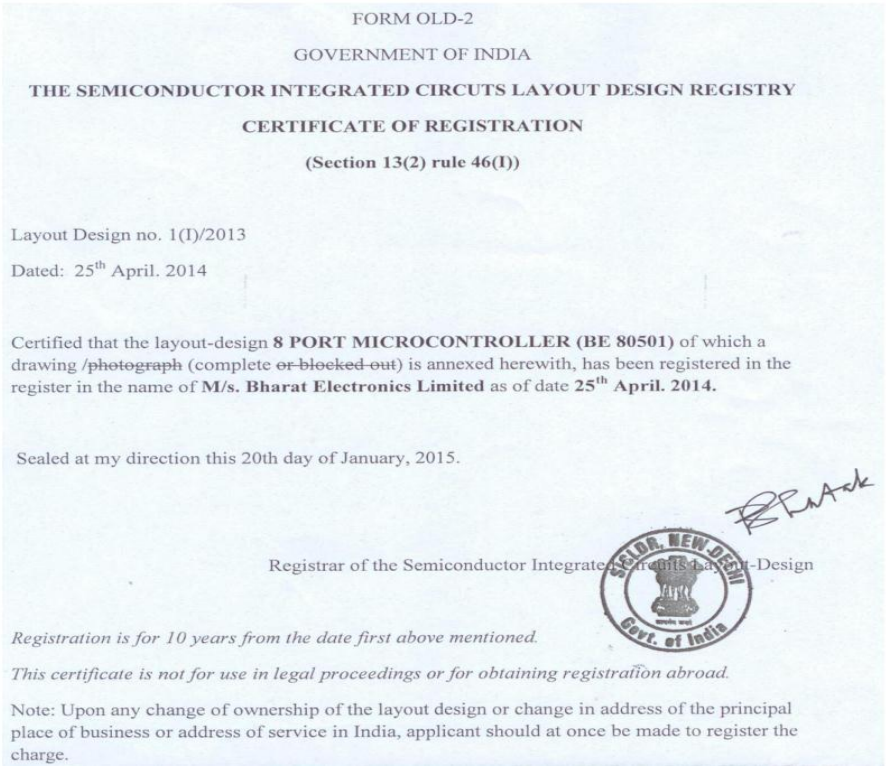
- A copy of the counter statement provided to the opposing party.
- The Registrar may take hearing with the parities.
- The Registrar will decide on the originality of the layout-design and grant or reject the application for registration based on the conclusions derived.
- Aggrieved party can appeal to Appellate Board or in its absence Civil Court for relief on any ruling of the Registrar.

  6)The registration of a layout-design shall be only for a period of ten years from the date of filing an application for registration as per section 15 of the Semiconductor Integrated Circuits Layout-Design Act, 2000.

  7) The owner of registered layout-designs has the exclusive right to use the layout-design and also enforce in case of any infringement. The right is available irrespective of the actual use of the layout-design in any article/good/product/device.

Certificate issued under **Semiconductor Integrated Circuits Layout Design Registry(SICLDR):**	
1) Title: 50-60 GHz Sub Harmonic IQ Mixer **Issued to:** M/s. Indian Space Research Organisation (ISRO) **Dated:** 24th May, 2016 **Design No.:** 2(I)/2016	**2) Title:** 8 port Micro-controller (BE.80501) **Issued to:** M/s. Bharat Electronics Ltd. (BEL) **Dated:** 20th January, 2015 **Design No.:** 1(I)/2013

Design No.: 2(I)/2016; **Title:** 8 port Micro-controller(BE.80501); **Issued to:** M/s. Bharat Electronics Ltd. (BEL); **Dated:** 20th January, 2015; **Design No.:** 1(I)/2013



FORM OLD-2

GOVERNMENT OF INDIA

THE SEMICONDUCTOR INTEGRATED CIRCUTS LAYOUT DESIGN REGISTRY

CERTIFICATE OF REGISTRATION

(Section 13(2) rule 46(I))

Layout Design no. 1(I)/2013

Dated: 25th April. 2014

Certified that the layout-design **8 PORT MICROCONTROLLER (BE 80501)** of which a drawing /~~photograph~~ (complete ~~or blocked out~~) is annexed herewith, has been registered in the register in the name of **M/s. Bharat Electronics Limited** as of date **25th April. 2014.**

Sealed at my direction this 20th day of January, 2015.

Registrar of the Semiconductor Integrated Circuits Layout-Design

Registration is for 10 years from the date first above mentioned.

This certificate is not for use in legal proceedings or for obtaining registration abroad.

Note: Upon any change of ownership of the layout design or change in address of the principal place of business or address of service in India, applicant should at once be made to register the charge.

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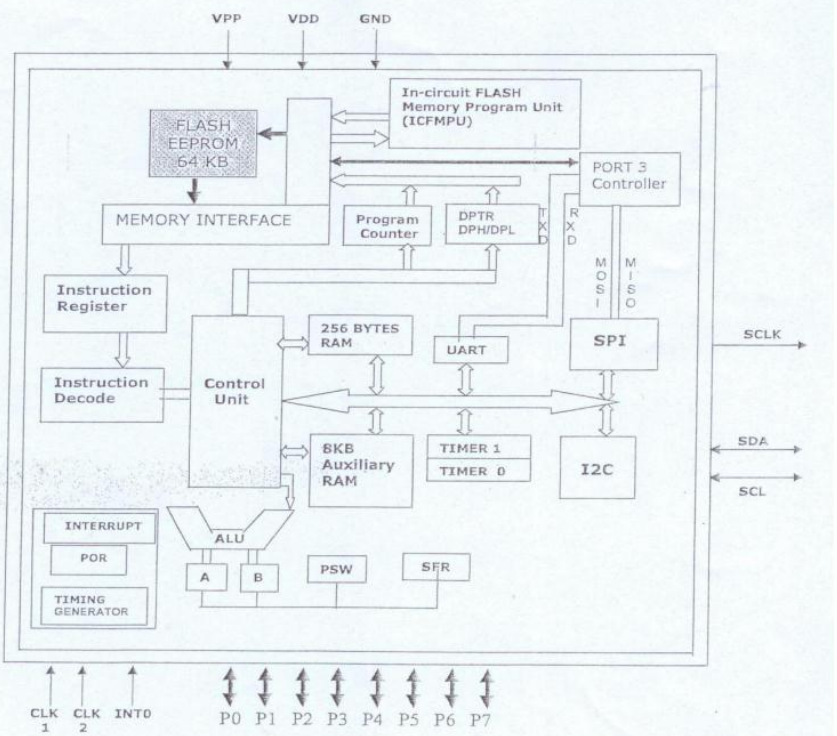
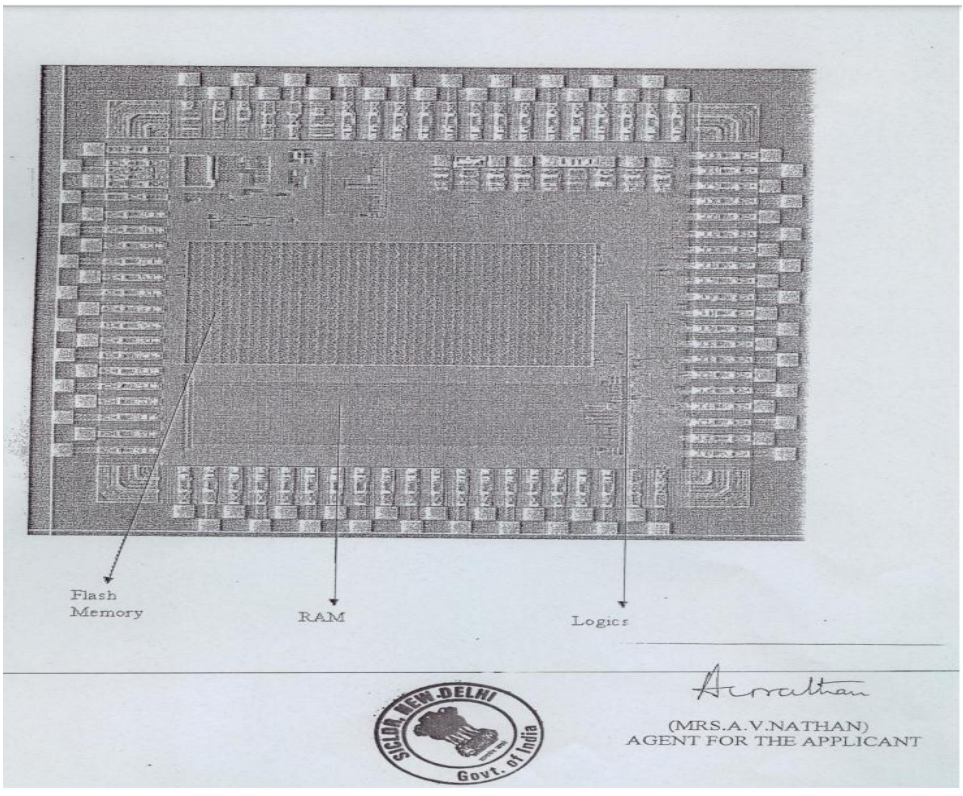
8 Port Microcontroller

Schematic diagram of functional blocks



(MRS.A.V.NATHAN)
AGENT FOR THE APPLICANT



(MRS.A.V.NATHAN)
AGENT FOR THE APPLICANT

Enforcement

The civil remedies, such as injunctions; the account of profits and damages would be applicable to enforce rights with respect to layout-designs. As per Section 16 of the Act,no person shall be entitled to institute any proceeding to prevent, or to recover damages for infringement of an unregistered layout-design.

Any person who contravenes knowingly andwilfully any of the provisions of Section 18of the Act, shall be punishable with imprisonment for a term which mayextend to three years, or with fine which shall not be less than fifty thousand rupees but which may extendto ten lakh rupees, or with both as per Section 56 of the Act.

The Infringement of layout-design provisions under Section 18of the Act is defined as "A registered layout-design is infringed by a person who, not being the registered proprietor of the layout-design or a registered user thereof,(a) Does any act of reproducinga registered layout-design in its entirety or any part thereof; (b) Does any act of importing or selling or otherwise distributing for commercial purposes a registered layout-design oran article incorporating such a semiconductor integrated circuit containing such registered layout-design for the use of which such person is not registered proprietor".

However, the performance of the act for the limited purposes of scientific evaluation, analysis, research or teaching, shall not constitute act of infringement within the meaning of that clause. But when a person, on the basis of scientific evaluation or analysis of a registered layout-design, creates another layout-design which is original; that person shall have the right to incorporate such another layout-design in a semiconductor integrated circuit or to perform any of the acts in respect of such another layout-design. This type of creation and its incorporation is not regarded as infringement as per the law.

As per Section 28 of the Act, right of registered user to take proceedings against infringement: Subject to any agreement subsisting between the parties, a registered user may make complaint before the competent criminal court for the infringement in his own name as if he were the registered proprietor.

MEMS (IC layout design) industrychallenges:

Some of the major challenges facing the MEMS/IC layout design industry include:

- Access to Foundries: Micro-Electro-Mechanical Systems(hereinafter referred to as "MEMS" companies today have very limited access to IC layout design fabrication facilities, or foundries, for prototype and device manufacture.
- Packaging and Testing: The packaging and testing of devices is probably the greatest challenge facing the MEMS industry.

Government Scheme

Indian industry and institutes are still at the initial stage of fabrication of chip technology.In order to have registration and then enforcement of any intellectual property, it is necessary to have a obtain full awareness about related procedure and schemes of intellectual property right (IC layout design registration). So, for IP Protection in Electronics & IT (SIP-EIT) Scheme, Department of Electronics and Information Technology has launched a scheme, "Scheme to Support IPR Awareness Seminars/Workshops in E&IT Sector".Under this scheme, DeitY aims to provide financial support to Education Institutes, DeitY societies, etc. for organizing seminars & workshops on IPR awareness among various stakeholders.

Conclusion:

Innovations are the backbone of a knowledge economy and innovation is the primary keyfor intellectual property rights. This is essential for any progressing economy.

Creating a new layout design for an integrated circuit involves a major investment and lack of clarity with respect to the procedures and the timelines as well as enforcement is a major hurdle whereby this Intellectual property has remained at a back foot as compared to all other Intellectual property rights.Thus, despite the statutory act being in force since 2000 more than two decades have passed and only two designs have been registered under Semi-Conductor.Further, there is lack of IC design layout (MEMS:Micro-Electro-Mechanical Systems) industries and infrastructurefor implementation of this IP in India as of now. The layout designs of integrated circuits are creations of the human mind. Under Semiconductor Integrated Circuits Layout Design Act 2000,exclusive right to the Integrated circuit layout is granted intends to encourage creativity.

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